Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-18. (Canceled)

19. (Currently amended) A method executed in a processor comprising:

loading a first number N of bits from a second extended multimedia register ~~source~~ into a lower half of a 2N wide-bit first extended multimedia ~~destination~~ register and in a upper half of the 2N-bit wide first extended multimedia destination register.

20. (Currently amended) The method of claim 19 in which the second extended multimedia register ~~source~~ is a memory location and where N is 64 bits.

21. (Original) The method of claim 20 in which the memory location contains a double floating point data type.

22. (Currently amended) The method of claim 19 in which the second extended multimedia register ~~source~~ is a 128-bit source register and N is 64 bits.

23. (Original) The method of claim 19 in which the 128-bit source register contains a double floating point data type.

Claims 24-72. (Canceled)

73. (Currently amended) A processor comprising:

basic program registers;

an address space;

floating point unit (FPU) registers;

single instruction multiple data (SIMD) extension registers;

a first extended multimedia ~~source~~ register;

a second extended multimedia ~~destination~~ register; and

logic to load a first portion of bits of the second extended multimedia ~~source~~ register into a first portion of the first extended multimedia ~~destination~~ register and duplicate that first portion of bits in a subsequent portion of the first extended multimedia ~~destination~~ register.

74. (Currently Amended) The processor of claim 73 in which the first portion of the second extended multimedia ~~source~~ register is 64-bits representing a double floating point data type in a memory location.

75. (Currently Amended) The processor of claim 73 in which the first portion of the second extended multimedia ~~source~~ register is 64-bits representing a double floating point data type in another source register.

76. (Currently Amended) The processor of claim 73 in which the first portion of the first extended multimedia ~~destination~~ register is loaded with bits [63-0] of the first portion of the second extended multimedia ~~source~~ register and the subsequent portion of the first extended multimedia ~~destination~~ register is loaded with bits [63-0] of the first portion of the second extended multimedia ~~source~~ register.

77. (Currently Amended) A processor comprising:

basic program registers;

an address space;

floating point unit (FPU) registers;

single instruction multiple data (SIMD) extension registers;

a ~~source~~ first extended multimedia register;

a ~~destination~~ second extended multimedia register; and

logic to load 64-bits of the ~~source~~ second extended multimedia register and return the 64-bits in a lower half of the ~~destination~~ first extended multimedia register and a upper half of the destination register.

78. (Previously presented) The processor of claim 77 in which the logic comprises:

a source operand; and

a destination operand.

79. (Previously presented) The processor of claim 78 in which the source operand is a memory location.

80. (Previously presented) The processor of claim 79 in which the memory location has a 128-bit value that represents a double floating point data type.

81. (Previously presented) The processor of claim 79 in which the source operand is a 128-bit source register.

82. (Previously presented) The processor of claim 81 in which the 128-bit source register has a 128-bit value that represents a double floating point data type.